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# 6. Cost and Emission Reduction Analysis of PFC, HFC, and SF<sub>6</sub> Emissions from Semiconductor Manufacturing in the United States

### 6.1 Introduction

The semiconductor industry uses multiple long-lived fluorinated gases in plasma etching and chemical vapor deposition (CVD) chamber cleaning processes. The gases most often used are trifluoromethane (HFC-23), perfluoromethane (CF<sub>4</sub>), perfluoroethane (C<sub>2</sub>F<sub>6</sub>), and sulfur hexafluoride (SF<sub>6</sub>), although other compounds such as nitrogen trifluoride (NF<sub>3</sub>), perfluoropropane (C<sub>3</sub>F<sub>8</sub>) and perfluorocyclobutane (C-C<sub>4</sub>F<sub>8</sub>) are also used. The four most common compounds respectively have 11,700; 6,500; 9,200; and 23,900 times the 100-year GWP of carbon dioxide. The weighted industry average of these four is 9,000 based on emissions of each. In the absence of emission control measures, the rapid growth in this industry (historically 15 percent per year in the mid-1990s) combined with the increasing complexity of microchips would be expected to result in increased future emissions of byproducts such as perfluorocarbons (PFCs), hydrofluorocarbons (HFCs), and SF<sub>6</sub>. While the exact combination of the four above compounds used is specific to the process employed and the type of product being manufactured, the total PFC, HFC, and SF<sub>6</sub> emissions from semiconductor manufacturing in the U.S. is expected to reach over 17 MMTCE by 2010, as shown in Exhibit 6.1. Actual emissions are likely to be much lower as a result of emission mitigation actions by industry, which are not included in this business-as-usual scenario forecast.

In 1996, EPA launched the PFC Emission Reduction Partnership for the Semiconductor Industry. This is a voluntary partnership with U.S. semiconductor producers with the goal of developing ways to reduce the emissions of high GWP gases used in semiconductor manufacture. In 1998, EPA and U.S. manufacturers began working with governments and producers in Europe, Japan, Korea, and Taiwan to develop a global strategy to reduce PFC emissions from semiconductor manufacture. In 1999, the World

Emissions from Semiconductor Manufacture 21% (17.5 MMTCE) 2010 Emissions 20.0 from Semiconductor Manufacture 18.0 16.0 14.0 100-Year GWP 12.0 9,000 (weighted avg.) 10.0 8.0 6.0 4.0 2.0 Total 2010 U.S. High GWP Gas Emissions:

Exhibit 6.1: U.S. Historical and Baseline HFC, PFC and SF<sub>6</sub> Emissions from Semiconductor Manufacture

84.2 MMTCE (assumes no further actions)1

0.0

<sup>&</sup>lt;sup>1</sup> An explanation of the business-as-usual scenario under which baseline emissions are estimated appears in the Introduction to the Report.

Semiconductor Council set a voluntary goal of reducing emissions to 10 percent below 1995 levels by 2010. This voluntary target covers over 90 percent of global semiconductor production. Neither global nor U.S. cost estimates for meeting this target have been completed, but significant investments are expected to meet the goal. Initially, technical innovations introduced by industry are likely to lead to major overall cost reductions in semiconductor manufacturing.

Semiconductor manufacturing is a high growth and rapidly changing industry. Despite this growth, however, total emissions from this industry may peak, according to some reports, by the year 2005 as a result of emission reduction efforts. This represents a substantial reduction in emissions, as much as 50 percent by some estimates, from what would have been released if the industry had expanded production without addressing PFC and other high GWP gas emissions.

### 6.2 Historical and Baseline HFC, PFC, and SF<sub>6</sub> Emission Estimates

Baseline emissions of high GWP gases from U.S. semiconductor manufacturing were estimated to be 1.5 MMTCE in 1995 (Exhibit 6.2). This estimate was developed based on the approximate sales of the four main gases (HFC-23, CF<sub>4</sub>, C<sub>2</sub>F<sub>6</sub>, and SF<sub>6</sub>) to semiconductor firms. Estimates were confirmed with data reported to the EPA by a subset of firms in the industry who have engaged in voluntary emissions reporting efforts. Emissions for the years 2000, 2005, and 2010 were estimated based on projections of historical trends in PFC usage, PFC emissions, and silicon consumption in semiconductor manufacturing, and are presented in Exhibit 6.3.

 $NF_3$  use is rapidly gaining market share in the semiconductor industry for CVD chamber cleaning because of its high process efficiency. Though a greenhouse gas,  $NF_3$  was not listed with a GWP in the IPCC's Second Assessment Report (Molina et al., 1995). This analysis presents options being considered by the semiconductor industry to reduce emissions of greenhouse gases, including  $NF_3$ . The business-as-usual estimate includes projected baseline emissions of  $NF_3$ . The semiconductor industry uses a broader definition of the term "PFC"—perfluorocompound, rather than perfluorocarbon—and therefore includes  $NF_3$  when referring to PFC emissions. The term "FC" will be used in this section to describe fluorinated compounds used as of 1995 (HFC-23,  $CF_4$ ,  $C_2F_6$ , and  $SF_6$ ) and  $NF_3$  will be discussed independently, to remain consistent with the remainder of this report.

| Exhibit 6.2: Historical U.S. HFC, PFC, and SF <sub>6</sub> Emissions from Semiconductors (1990-1999) |      |      |      |      |      |      |      |      |      |      |
|--|------|------|------|------|------|------|------|------|------|------|
|  | 1990 | 1991 | 1992 | 1993 | 1994 | 1995 | 1996 | 1997 | 1998 | 1999 |
| Emissions (MMTCE)  | 0.8  | 0.8  | 0.8  | 1.0  | 1.2  | 1.5  | 1.9  | 1.9  | 1.9  | 1.9  |
| C FDA 2001   |      |      |      |      |      |      |      |      |      |      |

Source: EPA, 2001.

Note: Conversion to MMTCE is based on the GWPs listed in the Introduction to the Report.

| Exhibit 6.3: Baseline U.S. HFC, PFC, NF <sub>3</sub> and SF <sub>6</sub> Emissions from Semiconductors (2000-2010) |      |      |      |  |  |
|--|------|------|------|--|--|
|  | 2000 | 2005 | 2010 |  |  |
| Emissions (MMTCE)  | 3.1  | 8.7  | 17.5 |  |  |

Notes:

Forecast emissions are based on a business-as-usual scenario, assuming no further action.

NF<sub>3</sub> was assumed to account for one percent of total emissions from semiconductor manufacturing based on 1995 gas usage. Conversion to MMTCE is based on the GWPs listed in the Introduction to the Report.

## 6.3 HFC, PFC, and SF<sub>6</sub> Emission Reduction Opportunities

Opportunities to reduce emissions from semiconductor manufacturing fall into the following three categories: CVD cleaning emission reduction technologies (*in situ* dilute NF<sub>3</sub> clean technology and NF<sub>3</sub> remote cleaning technologies), etching emission reduction technologies (plasma abatement, thermal destruction and catalytic destruction) and facility-wide solutions (recapture/recycling and process optimization). Costs (cost-of-ownership) and technical feasibility of implementation vary depending on the products manufactured (product type and size of wafer processed) and the design and age of the fabrication facility (fab). Existing fabs (capable of processing wafers up to 200 millimeters in diameter) may have insufficient infrastructure and space to implement some emission reduction technologies. For new and future planned fabs, purchasing state-of-the-art process equipment (much of which is still in the design phase) that optimizes PFC use and employs alternative chemistries is currently believed to be the least-cost option. The following outlines some of the commercially available or near commercially available technologies.

### **CVD Cleaning Emission Reduction Technologies**

Current and historical semiconductor manufacturing processes use  $C_2F_6$  as the primary dry chamber clean gas. The industry has developed NF<sub>3</sub>-based clean recipes that may be used to safely and efficiently clean CVD chambers in place of traditional  $C_2F_6$ . Two basic NF<sub>3</sub> clean technologies are currently available—one that introduces NF<sub>3</sub> directly into the CVD process chamber (*in situ*) where the gas is dissociated in a plasma; and another which dissociates NF<sub>3</sub> in a plasma upstream (remote) of the CVD process chamber and sends the active N and F atoms to selectively clean deposited material from inside the chamber. While NF<sub>3</sub> possesses a GWP marginally lower than  $C_2F_6$  (8,000 vs. 9,200), it is the chemical's overall efficiency that leads to the reduced climate impact as compared to  $C_2F_6$ , in that less NF<sub>3</sub> is needed to perform the same function and the gas is reacted more fully.

*In situ* NF<sub>3</sub> Clean Technology (Novellus). *In situ* NF<sub>3</sub> has been demonstrated to achieve emission reductions of greater than 90 percent at all process conditions. A plasma is generated inside the chamber by dissociating the NF<sub>3</sub> molecules, whose products then remove deposits to produce predominantly HF and other compounds that are removed by a facility's acid gas scrubber system.

NF<sub>3</sub> Remote Clean<sup>TM</sup> Technology (Applied Materials). The Remote Clean<sup>TM</sup> NF<sub>3</sub> system has been demonstrated to reduce FC emissions from the dielectric chamber cleaning process by over 95 percent. The unit uses an upstream device to dissociate NF<sub>3</sub> using argon gas at a 99 percent efficiency rate. In addition, chamber cleaning times are 30 to 50 percent faster than baseline C<sub>2</sub>F<sub>6</sub> clean times (International SEMATECH, 1999). The Remote Clean<sup>TM</sup> system converts the source gas to active atoms in the plasma, upstream of the process chamber. These electrically neutral atoms can selectively remove material in the chamber. The remote cleaning technology differs from *in situ* technology in that the NF<sub>3</sub> dissociates into plasma before entering the chamber rather than being dissociated inside the chamber. The byproducts of Remote Clean<sup>TM</sup> include HF, F<sub>2</sub>, and other gases, of which all but F<sub>2</sub> are removed by facility acid scrubber systems.

### **Etching Emission Reduction Technologies**

**Point-of-Use Plasma Abatement (Litmas).** The point-of-use plasma abatement system uses a small plasma source which can be located in the foreline of an etch tool or in the gas line between the process tool and the main pump, thus isolating the tool from the fab's waste stream. This plasma system is located before the dry pump nitrogen purge such that it can access the undiluted exhaust stream. It effectively dissociates the FC molecules, which react with fragments of the additive gas—H<sub>2</sub>, O<sub>2</sub>, H<sub>2</sub>O, or CH<sub>4</sub>—in order to produce low molecular weight by-products such as HF with little or no GWP. Wet scrubbers can then remove these product molecules. The presence of additive gas is necessary to prevent later

downstream reformation of FCs (Motorola, 1998). Plasma abatement has been shown to reduce emissions from the etcher by over 97 percent when using water vapor as an additive gas (International SEMATECH, 1998c). The evaluations performed to date indicate no apparent interference with the etch process.

Thermal Destruction/Thermal Processing Units (TPU). This technology can be used to reduce PFC emissions from both the etching and the CVD chamber cleaning process and is advantageous in that it does not affect the manufacturing process (Applied Materials, 1999a). Several commercially available FC thermal destruction systems can effectively abate some FCs, but only a few have been proven to abate all FCs at greater than 90 percent destruction efficiency. In addition, the combustion devices require a combustion fuel and use significant amounts of cooling water that creates wastewater, requiring treatment as industrial waste. Thermal oxidation may also produce  $NO_x$  emissions, which are regulated air pollutants.

Catalytic Decomposition System (Hitachi). Catalytic destruction systems are similar to thermal destruction units in that the system is installed in the process after the turbo pump that dilutes the exhaust stream prior to feeding it through the scrubber and emitting the scrubbed gases into the atmosphere. Consequently, there is no back-flow into the etching tool itself, which could adversely affect the performance of the etching tool. Catalytic destruction technologies can reduce FC emissions by 98 percent. However, their design must reflect a minimum concentration and flow of FC within the exhaust stream. Therefore, off-the-shelf systems will work only for facilities with certain stream or process specifications. Because catalytic destruction systems operate at low temperatures, they produce little or no NO<sub>x</sub> emissions and have low water demands.

### **Fab-Wide Solutions**

**PFC Capture/Recovery.** This technology separates unreacted and/or process-generated FCs from other gases for further processing. Currently available capture systems are guaranteed to remove 90 percent of emissions. In general, removal efficiency of C<sub>2</sub>F<sub>6</sub>, CF<sub>4</sub>, SF<sub>6</sub>, and C<sub>3</sub>F<sub>8</sub> is higher, in the high 90s, while CHF<sub>3</sub> and NF<sub>3</sub> removal efficiencies fall between 50 to 60 percent. For this analysis, an average figure of 90 percent is used (Kelly, 1999). This effluent treatment process allows for the possibility of some recycling or reuse of the captured FC gas (Mocella, 1998). These systems can either repurify the FC for reuse or they can concentrate the gas for subsequent offsite disposal. Semiconductor manufacturing exhaust requires considerable pretreatment to remove materials undesirable to the separation technology. Because current demand for recycled FCs is low, either destruction or reprocessing must be considered (Mocella, 1998). Destruction costs are estimated to be \$3/kilogram. Reprocessing costs are estimated to be significantly more expensive so this option is not considered further here. Although a few companies have installed pilot FC capture/recovery systems, this technology is reported to be unattractive if NF<sub>3</sub> cleaning systems are used because such cleaning processes do not leave sufficient FCs in the stream to make gas recovery economically viable.

**Lower GWP Substitutes.** This practice has the potential to reduce FC emissions from semiconductor manufacturing by replacing conventionally used FCs with other FCs that yield comparable performance with less potential environmental impact due to lower GWPs, high destruction efficiency, or lower atmospheric lifetimes. For example, in the etching process, the currently used FC C-C<sub>4</sub>F<sub>8</sub> has a GWP of 8,700. In contrast, alternatives such as  $C_3F_6$  and  $C_5F_8$  create approximately equal contact holes and have respective GWPs of 90 and 100. In addition,  $C_5F_8$  has an atmospheric lifetime of one year and a destruction efficiency of greater than 90 percent, versus a lifetime of 3,200 years and a destruction efficiency of about 80 percent for  $C_4F_8$  (Cowles, 1999; Hokari, 1999). These substitutes may have faster or comparable etching rates, increased etching efficiency, and may lead to an overall reduction in amount of FCs used and emitted for each process type. (Varying byproduct emissions—the small fraction of each FC used that is transformed into  $CF_4$ —present an additional concern to be factored into estimates of the

overall potential reductions that may result from substitution.) Although FCs are not completely eliminated in these cases, overall emissions and potential impacts may be lower than in a scenario without the substitution. Because cost estimates are unavailable at this time, this option is not discussed further.

**Process Optimization.** This practice involves the use of end-point detectors and/or process parameter variation to find the level of optimum FC utilization to reduce excess emissions. For example, optimization using  $C_2F_6$  in the chamber cleaning processes has been reported to reduce consumption by up to 50 percent and to abate up to 85 percent of FC emissions, as well as reduce chamber cleaning times by 15 percent (Deacon 1997, Lagan *et. al.* 1997, McNabb 1997). Because cost estimates are unavailable at the present time, this option is not discussed further.

# 6.4 Cost Analysis

Cost analyses are conducted for the following options: NF<sub>3</sub> cleaning technologies, plasma abatement, thermal and catalytic destruction, and recapture/recovery. Process optimization and lower GWP substitutes were not considered due to lack of operational test data. Unless otherwise noted, the analyses are based on the assumption that U.S. semiconductor fabs use between 75,000 to 150,000 pounds of FCs per year. Using an emission factor of 0.6 to 0.8 pounds of FCs out for each pound in leads to an annual emissions range of 45,000 to 120,000 pounds per year. For the purposes of this analysis, it is assumed that 60 percent of the emissions are from the chamber cleaning process, and the other 40 percent come from the etching process on a mass basis.

Costs of implementing reduction technologies are fab specific, so they may differ from the information assumed below. A discounted cash flow analysis was performed for each emission reduction option to estimate the price of carbon equivalent that would offset the cost of implementing the emission reduction option using a project lifetime of five years and two discount rates of four and eight percent. Only the higher cost estimates are given for each reduction option to present the highest cost of mitigation scenario. Preliminary estimates of the potential emission reduction for each technology or practice by end use were also developed. These potential emission reductions are expressed as a percent reduction of 2010 baseline emission estimates.

### CVD Cleaning Emission Reduction Technologies

 $NF_3$  Remote Clean<sup>TM</sup> Technology (Applied Materials). The costs and emission reductions for implementing  $NF_3$  cleaning technologies are as follows:

- Total costs equal approximately \$95,000 per tool per year, which includes capital and operations/maintenance (O&M) costs; and
- Emission reductions are estimated to be 5,500 metric tons of carbon equivalent (TCE). The remote clean technology uses approximately 1,400 pounds of NF<sub>3</sub>/year, with an emission factor of approximately one percent (GWP 8,000). The business-as-usual cleaning technology would require approximately five times the amount of material by weight, thus replacing approximately 7,000 pounds of C<sub>2</sub>F<sub>6</sub>/year, with an emission factor of 70 percent (GWP 9,200).

*In situ* NF<sub>3</sub> Clean Technology (Novellus). There is currently no cost information available on the *in situ* Novellus Clean Technology. However, it is assumed that the cost will be no more expensive than the NF<sub>3</sub> remote cleaning technology. Therefore, the same cost of reduction and market share was used.

### **Etching Emission Reduction Technologies**

**Point-of-Use Plasma Abatement (Litmas).** The cost and emission reduction estimates for plasma abatement systems assume four chambers per tool and one tool. The costs and emissions reductions are as follows:

- Total costs equal approximately \$24,000 per year, which includes capital, O&M, and installation costs:
- Emission reductions are estimated to be 621 TCE. To estimate the potential reduction, it was assumed that C<sub>2</sub>F<sub>6</sub> has a flow of 100 cubic centimeters per minute; and
- An emission reduction of 261 kilograms per year per tool is expected based on the tool running for 650 hours/year with an abatement efficiency of 97 percent (Burton, 2000).

**Thermal Destruction System.** Currently available destruction systems can be used to reduce emissions. The cost and emission reduction estimates presented here assume 10 systems per facility. The costs and emission reductions are as follows:

- Total costs equal approximately \$2.1 to \$3.1 million per year, which includes capital, O&M, and installation costs; and
- Emission reductions are estimated to be 22,000 to 60,000 TCE.

**Catalytic Destruction.** Hitachi's catalytic destruction systems are a new technology and cost information was not available to the public. It is believed that the costs will be comparable to thermal destruction systems, but that emissions reduced will be higher by as much as 5,000 TCE.

#### **Fab-Wide Solutions**

**PFC Capture/Recovery or Recycling System.** Although several major gas suppliers have developed pilot PFC recapture/recovery systems, there is currently little or no market for the recovered material. However, in some instances where FCs must be used and NF<sub>3</sub> is not a possible substitute, recapture/recovery systems appear to be a technically viable means of reducing FC emissions. The cost estimate and emission reduction potential of this technology were based on the following assumptions:

- Total costs equal approximately \$1.8 million per year, which includes capital, O&M, and installation costs for two units per facility. Installation costs can vary considerably. One major cost is the installation cost for providing a segregated FC waste stream. For a new fabrication facility, this could range between \$600,000 to \$1,000,000, but could be much more for an older large facility;
- Emission reductions are estimated to be 50,000 to 134,000 TCE;
- Destruction costs are estimated to be \$3/kilogram or approximately \$1.10/TCE;
- Two systems are needed per facility; and
- It is assumed that FC recapture systems could be installed to accommodate up to half of all emissions from semiconductor manufacture. Thus, given the 90 percent average removal rate, up to 45 percent of emissions could be eliminated using FC recapture systems. Similarly, 45 percent could be eliminated by the destruction systems described above. These two options are mutually exclusive; manufacturers would implement either one or the other because using thermal destruction does not leave enough FCs in the stream to make recapture economically viable. As a result, the emission reductions estimated to be attainable from each option cannot be added together.

### Results

Exhibit 6.4 summarizes the options for reducing FC emissions from the semiconductor industry, their respective costs, and the associated incremental and cumulative emission reductions. Exhibit 6.5 shows the market assumptions used in calculating the reductions presented in Exhibit 6.4. Fab-wide reductions can be applied to 100 percent of the emissions, while etch and chamber specific reductions can only reduce emissions from their respective percentage of the total emissions. Plasma abatement is believed to be the most popular option in the industry at the moment, so it was given the largest percentage of reductions in the etching sector (55 percent). Recapture/recycling was given five percent of the etching sector and ten percent of the chamber cleaning sector. All other portions were given equal percentages of the remainder in the respective sectors.

| Exhibit 6.4: E | mission | Reduction | and | Cost | in | 2010 |
|----------------|---------|-----------|-----|------|----|------|
|----------------|---------|-----------|-----|------|----|------|

| Option                        | Break-even Cost (\$/TCE) Discount Rate |        | Incremental | Reductions | Sum of Reductions |         |  |
|-------------------------------|--|--------|-------------|------------|-------------------|---------|--|
|                               | 4%                                     | 8%     | MMTCE       | Percent    | MMTCE             | Percent |  |
| NF <sub>3</sub> In situ Clean | 17.51                                  | 18.57  | 4.7         | 27%        | 4.7               | 27%     |  |
| NF <sub>3</sub> Remote Clean  | 17.51                                  | 18.57  | 4.7         | 27%        | 9.4               | 53%     |  |
| Plasma Abatement              | 37.87                                  | 41.95  | 3.8         | 22%        | 13.1              | 75%     |  |
| Capture/Recycling             | 39.58                                  | 43.99  | 1.3         | 7%         | 14.4              | 82%     |  |
| Catalytic Destruction         | 127.29                                 | 141.93 | 1.4         | 8%         | 15.7              | 90%     |  |
| Thermal Destruction           | 138.61                                 | 154.54 | 1.3         | 7%         | 17.0              | 97%     |  |

Notes:

2010 baseline emissions from semiconductor manufacture equal 17.5 MMTCE.

Conversion to MMTCE is based on a GWP of 9,000.

Sums might not add to total due to rounding.

| Exhibit 6.5: Market Shares Used to Calculate Reductions from Semiconductor Manufacturing |                               |  |   |  |  |  |
|--|-------------------------------|--|---|--|--|--|
| Option   | Applicable<br>Process<br>Type | % of Industry to<br>Which the Option can<br>be Applied | % of Industry Process<br>Type Expected to Use<br>the Option | % of Total Reductions<br>Accounted for by Each<br>Option |  |  |
| Capture/Recycling  | Fab-wide                      | 100%   | 8%  | 8%   |  |  |
| Catalytic Destruction  | Etching                       | 40%  | 20%   | 8%   |  |  |
| Plasma Abatement   | Etching                       | 40%  | 55%   | 22%  |  |  |
| Thermal Destruction  | Etching                       | 40%  | 20%   | 8%   |  |  |
| NF <sub>3</sub> In situ Clean  | CVD                           | 60%  | 45%   | 27%  |  |  |
| NF <sub>3</sub> Remote Clean   | CVD                           | 60%  | 45%   | 27%  |  |  |

Notes:

This table assumes that chamber cleaning and etching processes account for 60% and 40%, respectively, of PFC emissions from semiconductor manufacturing.

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